IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
REQUEST FOR FILING (RULE 60) APPLICATION
For Design or Utility Applications

Rule 1.60 PATENT APPLICATION

[ ] Continuation)
)
[XX] Divisional)

of pending prior application of

Inventor(s): HWANG, Cheol-Sung

Parent Appln. Serial No.: 08/560,087

Parent Appln. Filed: November 17, 1995

DEPOSIT ACCOUNT NO. 19-0124
ATTY. DOCKET NO.: 647-2
GROUP ART UNIT: 2503
EXAMINER: Kelley, N.

DATE: March 12, 1997

Title: METHOD FOR FORMING LOWER ELECTRODE OF CAPACITOR

Hon. Assistant Commissioner
of Patents
Washington, D.C. 20037

Sir:

To effect the above-requested filing today:

1. Attached is a true copy of the prior application as originally filed, including:

   [X] Abstract;
   [X] Specification and claim(s) (unamended clean copy) as originally filed (**14** pages);
   [X] Signed declaration or oath as originally filed in prior application;
   [X] Drawings: **4** sheet(s)/set: [ ] 1 set informal; [X] 1 set formal of size [X] A4;

NOTE: No amendments (if any) referred to in the Oath/Declaration filed to complete the prior application introduced new matter.

2. [ ] This Rule 1.60 application is hereby filed by less than all of the inventors named in the prior application. Petition is hereby made requesting deletion as inventor(s) of the following who is/are not inventor(s) of the invention being claimed in this Rule 1.60 application:

   1.)
   2.)
   3.)
   4.)

3. [ ] Transfer the drawi[redacted]rom the prior application to this appli[redacted]on and abandon said prior application as of the filing date accorded this application. A third copy of this letter is attached for filing in the prior application file.

4. [X] Priority is claimed under 35 U.S.C. 119/365 based on filing in the Rep. of Korea of:

	Application No.	Filing Date
1.)	95-13694	29/MAY/1995
2.)		
3.)		

a. [ ] _____ (No.) Certified copy/copies attached.
b. [X] Certified copy/copies previously filed on November 17, 1995 in U.S. Application No. 08/560,087, filed on November 17, 1995.
c. [ ] Certified copy/copies filed during International stage of PCT/_____.
d. [ ] Priority is also claimed from PCT/_____filed _____.

5. [X] Prior application is assigned to: Samsung Electronics Co., Ltd. 416 Maetan-Dong, Paldal-Gu, Suwon-City, Kyungki-Do, Rep. Of Korea, by Assignment recorded on November 17, 1995 at Reel 7780, Frame -164.

6. [ ] Attached is an Assignment to Samsung Electronics Co., Ltd., 416 Maetan-dong, Paldal- gu, Suwon-city, Kyungki-do, Rep. of Korea.

Please return recorded Assignment to the address in item 8 below.

7. [X] The Power of Attorney in the prior application is to:

1.)	Charles R. Donohoe	Reg. No. 24,546
2.)	Neil A. Steinberg	Reg. No. 34,735
3.)	William L. Geary, Jr.	Reg. No. 35,879
4.)	Brian C. Altmiller	Reg. No. 37,271
5.)	Allen LeRoy Limberg	Reg. No. 27,211

whose address is indicated in item 8 below.

a. [X] The power appears in the original papers of the prior application.
b. [ ] Since the power does not appear in the original papers, a copy of the power in the prior application is attached.
c. [ ] Recognize as associate attorney:

1.)
2.)
3.)

8. Address all future communications to Samsung Electronics Co., Ltd., 1200 New Hampshire Avenue, N.W., Suite 550, Washington, D.C. 20036, Tel.: (202) 296-0227.

9. [**X**] Amend the specification by inserting before the first line the sentence:
--This is a [ ] continuation; [**X**] divisional of Application Serial No. 08/560,087, filed November 17, 1995.--

10. [**X**] Petition to extend the life of the above prior application to at least the date hereof
[ ] is being concurrently filed in that prior application.
[ ] was previously filed in that prior application.
[**X**] is not necessary for copendency.

11. [ ]The Examiner's attention is directed to both the second paragraph of guideline (2) in MPEP 609 and to the last paragraph of MPEP 2001.06(b) and to the submission in the prior application of the Information Disclosure Statement and document copies filed on _____.

12. [ ]Attached is a Rule 103 Petition to Suspend Action.

13. [**X**] **PRELIMINARY AMENDMENT to be entered before fee calculation**: (Do not make amendments here except for correction of improper multiple dependencies or cancellation of whole claims or multiple dependencies for purposes of reducing the filing fee per MPEP §§ 506 and 607; do not cancel all claims).

Please cancel claims 1-24 withour prejudice. (See attached Preliminary Amendment)

FILING FEE
THE FOLLOWING FILING FEE IS BASED ON
CLAIMS AS FILED AND CHANGED BY PRELIMINARY AMENDMENT IN ITEM 13

14. Basic filing fee for Utility Application, $770.00	$770.00	(PTO Code 101)
15. Total Effective Claims [4] minus 20 = ["0"] x $22 =	$	(PTO Code 103)
16. Independent Claims [1] minus 3 = ["0"] x $80 =	$	(PTO Code 102)
17. If any **proper** multiple claim remains, add $260.00	$	(PTO Code 104)
18. If "petition" box 12 above is X'd, add petition fee of $130.00	$	(PTO Code 122)
19. **TOTAL FILING FEE DUE:**	**$770.00**	

20. [ ] Attached:

21. **[XX]** Preliminary Amendment attached (to be entered after assigning Appln. No.)

22. [ ] The Following PRELIMINARY AMENDMENT is to be entered after assigning Application Number.

ADDITIONAL FEE CALCULATION FOR
PRELIMINARY AMENDMENT
PER BOXES 21 & 22

	Claims remaining after amendment		Highest number previously paid for		Present Extra		Additional Fee
23. Total Effective Claims:	**4**	(-)	**20**	=	x $22.00	$	(PTO Code 103)
24. Independent Claims	**1**	(-)	**3**	=	x $80.00	$	(PTO Code 102)
25. If amendment enters proper multiple dependent claim(s) into this application for first time, add $260.00						$	(PTO Code 204)
26.					Subtotal	$	
27.					Additional Fee	$	
28.					plus FEE from item 19 on page 3	$770.00	
29.					TOTAL FEE DUE	**$770.00**	

CHARGE STATEMENT: The Commissioner and Assistant Commissioner of Patents is hereby authorized to charge any fee specifically authorized hereafter, or any missing or insufficient fee(s) filed, or asserted to be filed, or which should have been filed herewith or concerning any paper filed hereafter, and which may be required under rules 16-18 (missing or insufficient fee only) now or hereafter relative to this application and the resulting Official document under Rule 20, or credit any overpayment to our Deposit Account/Order Nos. 19-0124, also shown in the heading hereof for which purpose a duplicate copy of this sheet is attached. THIS CHARGE STATEMENT does not authorize charge of the issue fee until/unless an issue fee transmittal form is filed.

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By Atty.: Brian C. Altmiller Reg. No. 37,271

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SEC-025 10/96

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re **DIVISIONAL** Application of

HWANG, Cheol-Sung

Group Art Unit: 2503

Parent Appln. Serial No. 08/560,087

Examiner: KELLEY, N.

Parent Appln. Filed: November 17, 1995

New Atty. Docket No. 647-2

Title: METHOD FOR FORMING LOWER ELECTRODE OF CAPACITOR

Assistant Commissioner of Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Prior to the Examination of the application referenced above, please consider the following amendments and remarks:

IN THE CLAIMS:

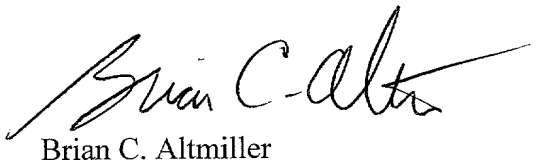
Please cancel claims 1-24 without prejudice or disclaimer.

REMARKS

In this Preliminary Amendment Applicant amends the specification by canceling claims 1-24 without prejudice or disclaimer. This application is a divisional application of U.S. Application Serial No. 08/560,087, which application contains canceled claims 1-24.

Applicants therefore request that the Examiner consider this amendment, enter the claim amendments, examine and consider and this application, and issue a Notice of Allowance allowing pending claims 25-28.

Respectfully Submitted,



Brian C. Altmiller
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Date: March 12, 19971

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APPLICATION FOR UNITED STATES PATENT

INVENTOR(S): HWANG, Cheol-sung

ENTITLED: Method For Forming Lower Electrode Of Capacitor

PRIORITY CLAIMED:

COUNTRY: Rep. of Korea

NO: 95-13694

FILED: May 29, 1995

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METHOD FOR FORMING LOWER ELECTRODE OF CAPACITOR

Background of the Invention

The present invention relates to a method for manufacturing a storage capacitor of a very large scale integrated (VLSI) semiconductor device. More particularly, the present invention relates to a method for forming the lower electrode of a capacitor to be used for fabricating a 1 Gbit or above dynamic random access memory (DRAM).

As DRAM device densities increase to 64 Mbits and above, the types of capacitors used in these devices have changed and must continue to change to meet a growing need for smaller capacitors with relatively large capacitances. To meet this growing need, conventional capacitors using NO (nitride and oxide) thin films as their dielectric layers have been developed using planar structures, trench structures, stack structures, cylinder structures, and fin structures to increase available capacitance. Of these structures, cylinder and fin capacitor types are limited in terms of economy and reliability due to their extremely complex structures and intricate fabrication methods.

Studies on the use of high-dielectric thin films to overcome problems incurred from the complexity of the required capacitor structure have been ongoing in the United States and Japan for the past ten years. From these studies, perovskite-structured materials such as barium titanium oxide ($BaTiO_3$), lead titanium oxide ($PbTiO_3$), strontium titanium oxide ($SrTiO_3$, or more simply, STO), lead zirconium titanium oxide ($Pb(Zr,Ti)O_3$) and barium strontium titanium oxide ($(Ba,Sr)TiO_3$, or more simply, BST) have attracted interest.

In particular, the very high dielectric constants of STO and BST materials (ranging from 300 to 600) make these materials appropriate for highly-integrated semiconductor capacitors. STO and BST materials allow for the simplification of capacitor processing in

VLSI semiconductor device applications such as DRAMs of more than 1 Mbit by allowing the use of capacitors with a simpler physical design. Because of the high dielectric constant of the material used in the dielectric layer, these capacitors can employ simple designs yet still obtain a sufficiently large capacitance.

A study on the application of capacitors having STO thin films as their dielectric films to 64 Mbit DRAMs has recently been conducted, as shown in H. Yamaguchi et al., "Structural and Electrical Characterization of $SrTiO_3$ Thin Films Prepared by Metal Organic Chemical Vapor Deposition," Japan Journal of Applied Physics, Vol. 32, Part 1, No. 913, pp. 4069-4073, (1993). When using the above dielectric films having high dielectric constants, the general-purpose polysilicon used with conventional NO and Ta_2O_5 thin films cannot be used as an electrode material. This is attributed to the susceptibility of polysilicon to oxidation during a thin film deposition process or subsequent thermal process because of the presence of a high dielectric film. If a low dielectric oxide layer is formed at the interface between the electrodes and the dielectric layer capacitance rapidly decreases, thus negating the beneficial effects of the high dielectric material.

Accordingly, when fabricating a capacitor with a high dielectric material, a lower electrode, on which a dielectric film is deposited, must be formed of a material which can withstand thermal processing. A noble metal that resists oxidation, such as platinum (Pt), or an oxide material, such as ruthenium oxide (RuO_2), have so far been used for the lower electrode when fabricating a capacitor with a high dielectric material. Pt and RuO_2 have their own advantages and disadvantages for use in the lower electrode of a high dielectric capacitor.

As is generally known, Pt is difficult to pattern into a storage node since it is a chemically stable metal. Although the possibility of patterning Pt by means of a variety of

gases is being explored, the problems of sidewall deposition of an etched object and low etch rate have yet to be solved.

RuO_2, in comparison, is easy to etch. However, the leakage current of an STO or BST film deposited on RuO_2 is about 100 times larger than if the same film were deposited on a Pt electrode. Despite its ease of etching, this large leakage current makes the use of RuO_2 unacceptable.

Summary of the Invention

The object of the present invention is to provide a method for forming the lower electrode of a high dielectric capacitor which is easy to manufacture and is electrically improved by manufacturing a storage node applicable to a 1 Gbit DRAM, taking advantage of the low leakage current properties of Pt and easy patterning of RuO_2.

To achieve the above object, there is provided a method for manufacturing a high dielectric storage capacitor of a high integrated semiconductor device, which includes a lower electrode, a highly dielectric film and an upper electrode, comprising the steps of: forming a first layer of the lower electrode over a substrate, the first layer comprising a material that serves as a barrier against the diffusion of impurities from the substrate; forming a second layer of the lower electrode over the first layer, the second layer comprising a material that is easy to pattern; and forming a third layer of the lower electrode over the second layer, the third layer comprising a material having low leakage current properties.

In more detail, the method for manufacturing a capacitor of the present invention comprises the steps of: forming an insulating film on a semiconductor substrate; forming a contact hole in the insulating film; forming a polysilicon plug in the contact hole; depositing a first layer over the contact hole, the first layer comprising a material that serves as a barrier

against the diffusion of impurities from the semiconductor substrate; depositing a second layer over the first layer, the second layer comprising a material that is easy to pattern; forming a hard mask pattern over the second layer; sequentially patterning the first and second layers; depositing a third layer over the patterned first and second, the third layer comprising a material having low leakage current properties; forming a dielectric layer on the third layer; and forming an upper electrode on the dielectric layer.

As a result of this manufacturing method there is provided a lower electrode of a capacitor in a semiconductor device, comprising a first layer comprising a material that serves as a barrier against the diffusion of impurities from a lower substrate; a second layer formed over the first layer, the second layer comprising a material that is easy to pattern; and a third layer formed over the second layer, the third layer comprising a material having low leakage current properties.

The first layer of the lower electrode preferably comprises TiN. The second layer of the lower electrode preferably comprises RuO_2. The third layer of the lower electrode preferably comprises Pt. The lower electrode, formed as a triple layer electrode, comprising the first, second, and third layers, is formed to be in contact with a dielectric layer. The dielectric layer is preferably a high-dielectric layer comprising a material from the group consisting of $SrTiO_3$ and $(Ba_xSr_{(1-x)})TiO_3$, and is preferably deposited by a CVD method.

The steps of depositing the first and second layers are preferably carried out through the use of a reactive DC sputtering process. The hard mask pattern preferably comprises silicon-on-glass (SOG) and the patterning step is preferably carried out through the use of a reactive ion etching method.

The step of depositing the third layer is performed by using a sputter method so that the third layer deposited over the top and sides of the first and second layers will have a

variable thickness. The third layer, deposited over the top of the first and second layers is preferably approximately 200Å thick.

The method for manufacturing a capacitor may further comprise a step of etching back the third layer to uniformly control the thickness of the third layer. When the third layer is overetched together with a portion of an interlayer insulating film formed below the third layer, this achieves complete isolation between node patterns during the step of etching back the third layer. The step of etching back the third layer is preferably controlled to maintain the thickness of the third layer on the top and sides of the node pattern at approximately 60Å.

According to a preferred embodiment of the present invention, a capacitor having a triple-layered lower electrode (or a storage node pattern) of Pt, RuO_2 and TiN is formed by forming an RuO_2 and TiN node pattern using RuO_2 which is easy to pattern, and depositing Pt having low leakage current properties on the top of the node pattern which is to be in contact with a high dielectric film. Therefore, the capacitor can be of great use in Gbit-DRAM applications.

Brief Description of the Drawings

The above objects and advantages of the present invention will become more apparent by describing in detail a preferred embodiment thereof with reference to the attached drawings in which:

Figs. 1 to 7 are cross-sectional views showing the steps in the formation of a capacitor lower electrode of a preferred embodiment of the present invention;

FIG. 8 is a cross-sectional photo showing the Pt thin film after the sputter deposition in a preferred embodiment of the present invention; and

FIG. 9 is a graph showing current density vs. applied voltage for explaining the leakage current characteristics of a capacitor manufactured according to a preferred embodiment of the present invention.

Detailed Description of a Preferred Embodiment of the Invention

FIG. 1 shows a step of forming contact holes on a semiconductor substrate 10, preferably a silicon substrate, on which an interlayer insulating film 12 is formed. For example, the contact holes are formed using a predetermined mask pattern after depositing the interlayer insulating film 12 on the semiconductor substrate 10 on which a sub-structure (not shown) is formed. The interlayer insulating film 12 is formed of, e.g., borophosphorous silica glass (BPSG), using a chemical vapor deposition (CVD) method or SiO_2 obtained by thermal oxidation of silicon.

FIG. 2 shows the steps of forming polysilicon plugs 14 in the contact holes. In these steps, the polysilicon is coated on the resultant structure to sufficiently fill the contact holes and then is etched back to form the polysilicon plugs 14.

FIG. 3 shows the steps of sequentially depositing a barrier layer 15 and a patterning layer 17 on the whole surface of the resultant using a DC sputter method. The barrier layer 15 is formed for the purpose of preventing the diffusion of silicon and impurities doped on conductive materials such as the semiconductor substrate 10 and the polysilicon plug 14 into the storage nodes. A metal nitride such as titanium nitride (TiN) is preferably used as a material for the barrier layer 15, although any suitable material that serves as a barrier against diffusion of impurities from the lower layers may be used. RuO_2 is preferably used for the patterning layer 17, although any suitable material that is easily patterned may be used.

FIG. 4 shows a step of forming a mask pattern 20 for creating storage node patterns, each of which is separated in units of a cell by etching the barrier layer 15 and the patterning layer 17. The mask pattern 20 is preferably a SOG hard mask and includes shapes corresponding to the polysilicon plugs 14.

FIG. 5 shows a step of sequentially patterning the barrier layer 15 and the patterning layer 17, preferably through an RIE method using the mask pattern 20. The storage node patterns are formed by anisotropically etching the surface of the parts of the barrier layer 15 and the patterning layer 17 that are exposed by the mask pattern 20. After etching, the storage node patterns of the patterning layer 27 and the storage node patterns of the barrier layer 25 are formed. The RIE process in the preferred embodiment is performed by using Cl_2 gas to etch the TiN and a mixture of Cl_2 and O_2 gases to etch the RuO_2. If materials other than TiN and RuO_2 are used for the barrier layer 15 and the patterning layer 17, suitable etching gases should be chosen. After the etching step, the mask pattern 20 is removed, preferably using a fluoroform gas (CHF_3). As mentioned above, RuO_2 and TiN are easy to etch. Accordingly, they have a process margin sufficient for application to 1 Gbit-scale patterns.

FIG. 6 shows a step of depositing a contact material, preferably Pt, on the storage node pattern of the patterning layer 27 and the storage node pattern of the barrier layer 25. A contact layer 19 is deposited on the top and sides of the barrier layer and patterning layer storage node patterns 25 and 27, and between these node patterns, through a sputtering process which leaves different thicknesses throughout the contact layer. The contact layer 19 preferably comprises a Pt thin film, although any suitable material having low leakage current properties may be used.

As noted above, the sputtering process produces poor step coverage. The sputtering method is used in the present invention to facilitate a later-described etch-back process in which horizontal etching is easy but vertical etching is difficult.

In the preferred embodiment it is desirable to control the Pt thin film contact layer 19 deposited on the tops of the node patterns to be approximately 200Å thick. The reason for this is based on the following experiment, which is described with reference to FIG. 8.

FIG. 8 shows a cross-sectional photo wherein Pt has been sputter-deposited over node patterns of SiO_2 instead of over RuO_2. For the DC sputtering, a DC power of 1.1KW and an argon (Ar) atmosphere of 6 mTorr were used. Various thicknesses were then measured as follows. The thickness of the top of the deposited Pt was approximately 1100Å. The thickness of the sides of the deposited Pt was about 300Å. The thickness between patterns was about 700Å.

The thickness of the super-thin film was determined to be 200Å based on the sputter-deposition property and the experimental result. This particular thickness is selected so that the separating distance between storage nodes in a 1 Gbit DRAM is narrow, e.g., about 1500Å, resulting in a limitation on the deposition thickness. Another reason is that when d1 is 200Å, d2 and d3 will be deposited to a thickness of approximately 60Å and 140Å, respectively, and about 60Å of Pt will remain on the top and sides by a subsequent etch-back process.

FIG. 7 shows an etch-back process for controlling the contact layer 19 to a uniform thickness. In the preferred embodiment, the Pt thin film contact layer 19 is sputter-deposited and electrically isolates the node patterns which are connected to one another. During the etch-back process, a mixture of Ar and Cl_2 gases are preferably used as a reactive gas for etching back of the contact layer 19. The process is controlled to form a contact thin film 29,

a Pt thin film in the preferred embodiment, which remains on the top and sides of the node pattern at a thickness of about 60Å. In the etch-back process of the preferred embodiment, the Pt deposited between the node patterns is preferably overetched, together with a portion of the interlayer insulating film 12 below the Pt layer, so that the nodes are entirely isolated from one another.

Through the above processes, the lower electrode of a high dielectric capacitor having a triple-layer is formed comprising a contact thin film 29, a patterning layer storage node pattern 27, and a barrier layer node pattern 25. The lowest layer of the triple-layer lowermost electrode, the barrier layer node pattern 25, is preferably formed of TiN or some other material that serves as a barrier against the diffusion of impurities from a lower substrate. The middle layer of the triple-layer lowermost electrode, the patterning layer node pattern 27, is preferably formed of RuO_2 or some other material that facilitates the production of fine patterns. The uppermost layer of the triple-layer lower electrode, the contact thin film 29 that is in contact with the high dielectric film, is preferably formed of Pt or some other material having low leakage current properties.

A formation step (not shown) of the high dielectric film on the contact thin film 29 is required for the creation of the desired capacitor. The dielectric film is formed on the upper layer 29 resultant, wherein the triple-layered lower electrode undergoes a deposition process of a dielectric material having a high dielectric constant such as STO. The deposition process is preferably performed by a metal organic CVD method at low temperature (about 450°C) in an oxygen atmosphere, accompanied by a thermal process thereafter.

Finally, a capacitor which is suitable for the next generation Gbit-DRAMs is manufactured by performing a formation process of an upper electrode on the high dielectric film.

The effects of the present invention will be more apparent by referring to FIG. 9, which illustrates J-V characteristic curves for explaining the leakage current property of the capacitor manufactured according to the present invention. The curves show the J-V characteristics of a conventional RuO_2 storage electrode and a storage electrode made of Pt, each of which has an STO dielectric film of 40nm deposited thereon. As shown in the graph of FIG. 9, the leakage current of the Pt electrode case (the X-curve of the graph) at a voltage of 1.5V is about $5x10^{-8}A/cm^{-2}$ and that of conventional technology (the Y-curve of the graph) is about $1x10^{-5}A/cm^{-2}$. The capacitor of the present invention can thus achieve a leakage current about 200 times lower than that of the conventional technology.

As described above, in the high dielectric capacitor of the preferred embodiment of the present invention, a triple-layered lower electrode of Pt, RuO_2 and TiN can be created by forming an RuO_2 and TiN storage node pattern and depositing Pt having a low leakage current property on the top of the node pattern to be in contact with the high dielectric film.

As a result, a high dielectric capacitor which has a high process margin and excellent electrical properties can be obtained. The capacitor technology of the present invention can be of great use in 1 Gbit or greater DRAM applications.

The present invention is not limited to the above-described embodiments. Various changes and modifications may be effected by one having an ordinary skill in the art within the scope of the invention as, defined by the appended claims.

What is claimed is:

1. A method for forming a lower electrode of a capacitor in a semiconductor device, including the steps of:

forming a first layer of the lower electrode over a substrate, the first layer comprising a material that serves as a barrier against the diffusion of impurities from the substrate;

forming a second layer of the lower electrode over the first layer, the second layer comprising a material that is easy to pattern; and

forming a third layer of the lower electrode over the second layer, the third layer comprising a material having low leakage current properties.

2. A method for forming the lower electrode of a capacitor according to claim 1, wherein the first layer of the lower electrode comprises TiN.

3. A method for forming the lower electrode of a capacitor according to claim 1, wherein the second layer of the lower electrode comprises RuO_2.

4. A method for forming the lower electrode of a capacitor according to claim 1, wherein the third layer of the lower electrode comprises Pt.

5. A method for forming the lower electrode of a capacitor according to claim 1, wherein the lower electrode is in contact with a dielectric layer.

6. A method for forming the lower electrode of a capacitor according to claim 5, wherein the dielectric layer is a high-dielectric layer comprising a material from the group consisting of $SrTiO_3$ and $(Ba_xSr_{1-x})TiO_3$.

7. A method for forming the lower electrode of a capacitor according to claim 5, wherein the dielectric layer is deposited by a CVD method.

8. A method for manufacturing a capacitor including the steps of:

forming an insulating film on a semiconductor substrate;

forming a contact hole in the insulating film;

forming a polysilicon plug in the contact hole;

depositing a first layer over the contact hole, the first layer comprising a material that serves as a barrier against the diffusion of impurities from the semiconductor substrate;

depositing a second layer over the first layer, the second layer comprising a material that is easy to pattern;

forming a hard mask pattern over the second layer;

sequentially patterning the first and second layers;

depositing a third layer over the patterned first and second, the third layer comprising a material having low leakage current properties;

forming a dielectric layer on the third layer; and

forming an upper electrode on the dielectric layer.

9. A method for manufacturing a capacitor according to claim 8, wherein the first layer comprises TiN.

10. A method for manufacturing a capacitor according to claim 8, wherein the second layer comprises RuO_2.

11. A method for manufacturing a capacitor according to claim 8, wherein the third layer comprises Pt.

12. A method for manufacturing a capacitor according to claim 8, wherein the steps of depositing the first and second layers are carried out through the use of a reactive DC sputtering process.

13. A method for manufacturing a capacitor according to claim 8, wherein the hard mask pattern comprises silicon-on-glass (SOG).

14. A method for manufacturing a capacitor according to claim 8, wherein the patterning step is carried out through the use of a reactive ion etching method.

15. A method for manufacturing a capacitor according to claim 8, wherein the dielectric layer comprises a high-dielectric film.

16. A method for manufacturing a capacitor according to claim 8, wherein the dielectric layer comprises a material from the group consisting of $SrTiO_3$ and $(Ba_xSr_{1-x})TiO_3$.

17. A method for manufacturing a capacitor according to claim 8, wherein the step of depositing the third layer is performed by using a sputter method so that the third layer deposited over the top and sides of the first and second layers will have a variable thickness.

18. A method for manufacturing a capacitor according to claim 17, wherein said third layer deposited over the top of the first and second layers is approximately 200Å thick.

19. A method for manufacturing a capacitor according to claim 18, further comprising a step of etching back the third layer to uniformly control the thickness of the third layer.

20. A method for manufacturing a capacitor according to claim 19, wherein the third layer is overetched together with a portion of an interlayer insulating film formed below the third layer, to achieve complete isolation between node patterns during the step of etching back the third layer.

21. A method for manufacturing a high dielectric capacitor according to claim 19, wherein step of etching back the third layer is controlled to maintain the thickness of the third layer on the top and sides of the node pattern at approximately 60Å.

22. A method for manufacturing a capacitor according to claim 8, further comprising a step of etching back the third layer to uniformly control the thickness of the third layer.

23. A method for manufacturing a high dielectric capacitor according to claim 22, wherein the third layer is overetched together with a portion of an interlayer insulating film formed below the third layer, to achieve complete isolation between node patterns during the step of etching back the third layer.

24. A method for manufacturing a high dielectric capacitor according to claim 22, wherein step of etching back the third layer is controlled to maintain the thickness of the third layer on the top and sides of the node pattern at approximately 60Å.

25. A lower electrode of a capacitor in a semiconductor device, comprising:

a first layer comprising a material that serves as a barrier against the diffusion of impurities from a lower substrate;

a second layer formed over the first layer, the second layer comprising a material that is easy to pattern; and

a third layer formed over the second layer, the third layer comprising a material having low leakage current properties.

26. A lower electrode of a capacitor according to claim 25, wherein the first layer comprises TiN.

27. A lower electrode of a capacitor according to claim 25, wherein the second layer comprises RuO_2.

28. A lower electrode of a capacitor according to claim 25, wherein the third layer comprises Pt.

Abstract of the Disclosure

A method for forming the lower electrode of a capacitor used for fabricating a 1-Gbit or above DRAM, using a material having a high dielectric constant, is used in a method for manufacturing a storage capacitor of a VLSI semiconductor device. The lower electrode, which is to be in contact with a high dielectric film, is formed to have a triple-structured storage node pattern. The lowest layer of the lower electrode is formed with TiN which serves as a barrier against the diffusion of impurities from a lower substrate. The middle layer of the lower electrode is formed with RuO_2 which is easy to pattern. The uppermost layer of the lower electrode is formed with Pt which has excellent leakage current properties.

FIG.1

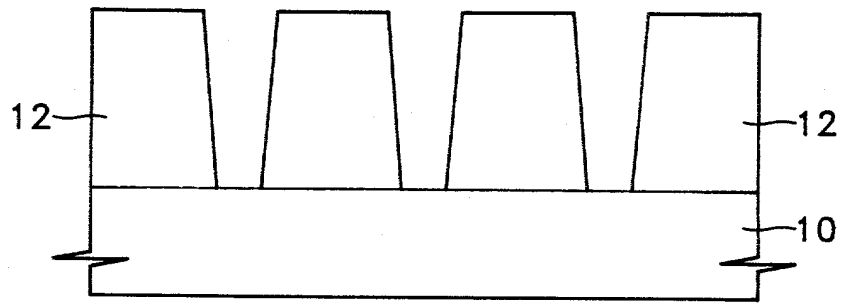


FIG.2

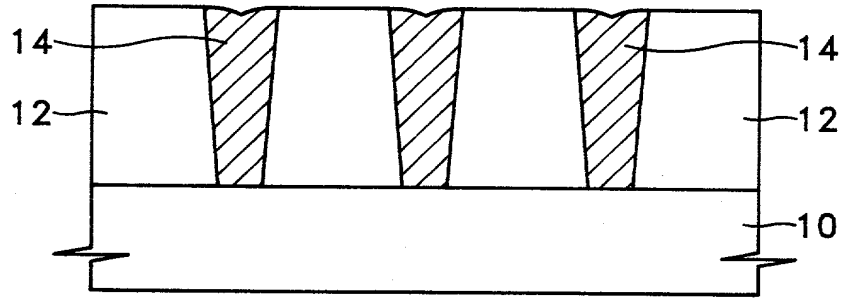


FIG.3

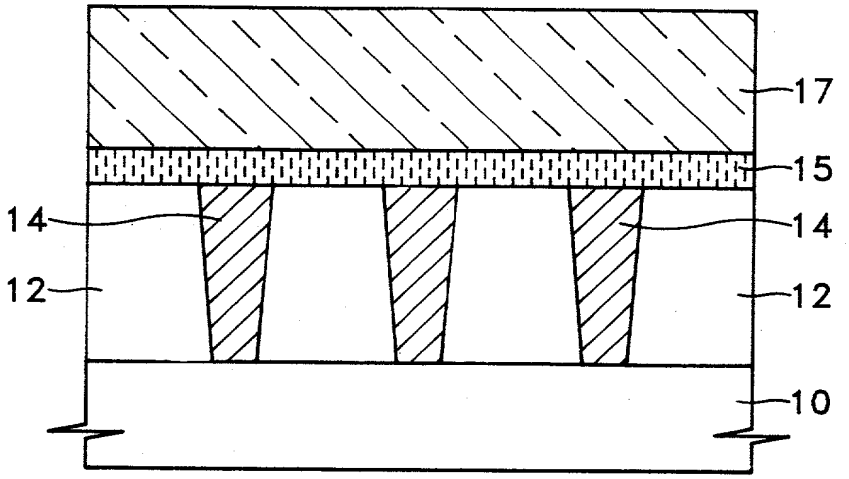


FIG.4

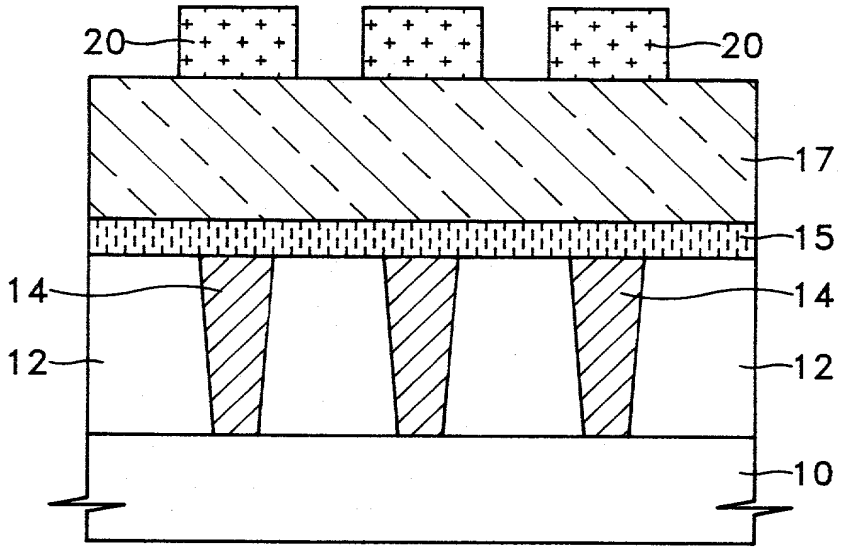


FIG.5

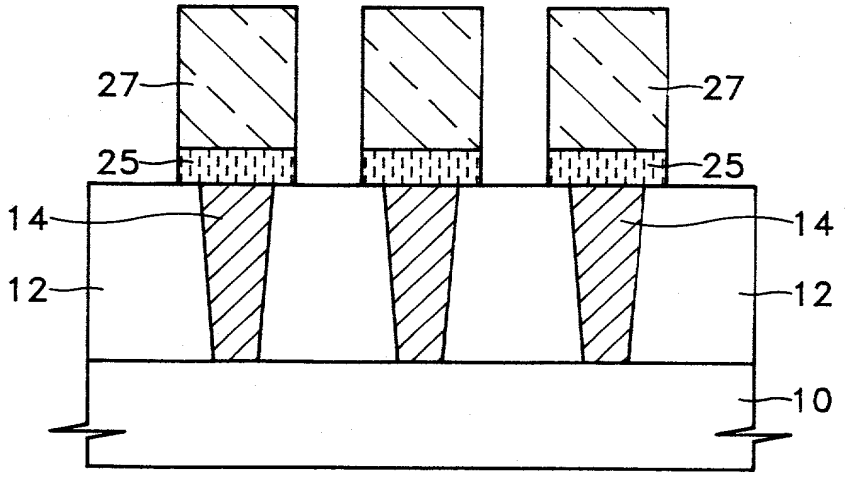


FIG.6

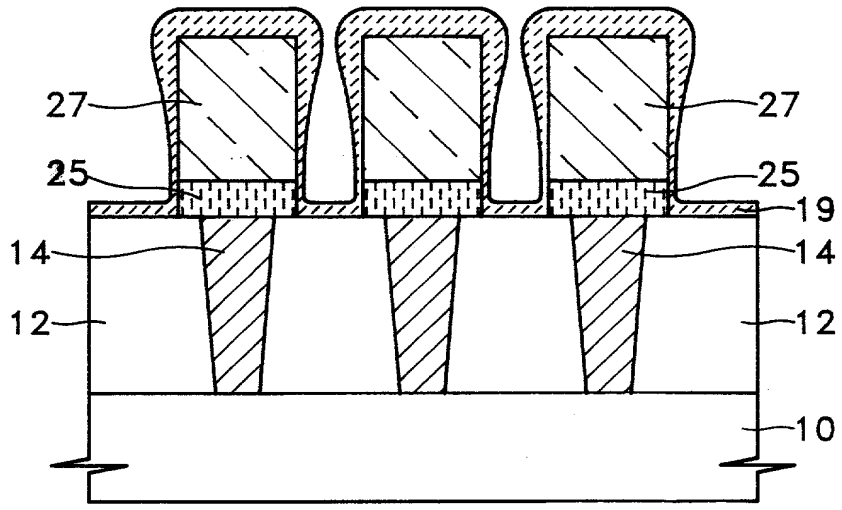


FIG.7

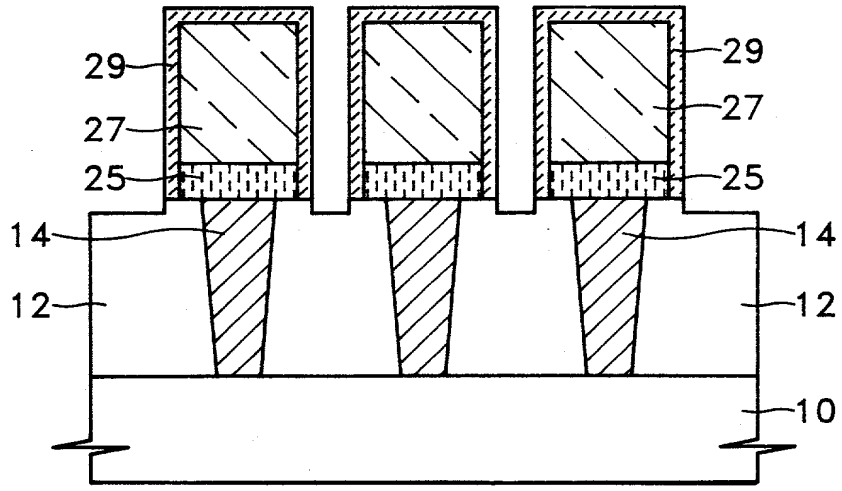


FIG.8

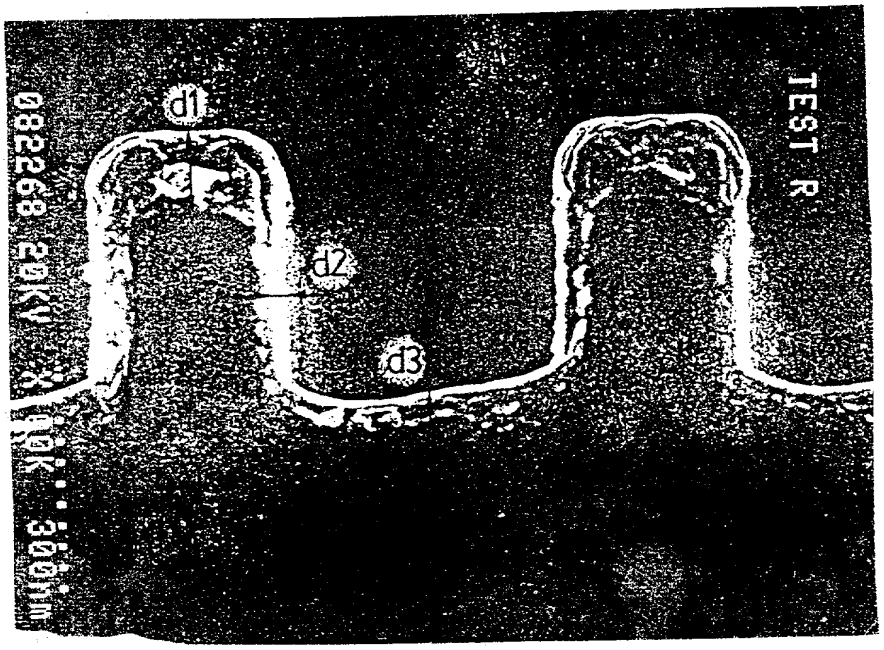
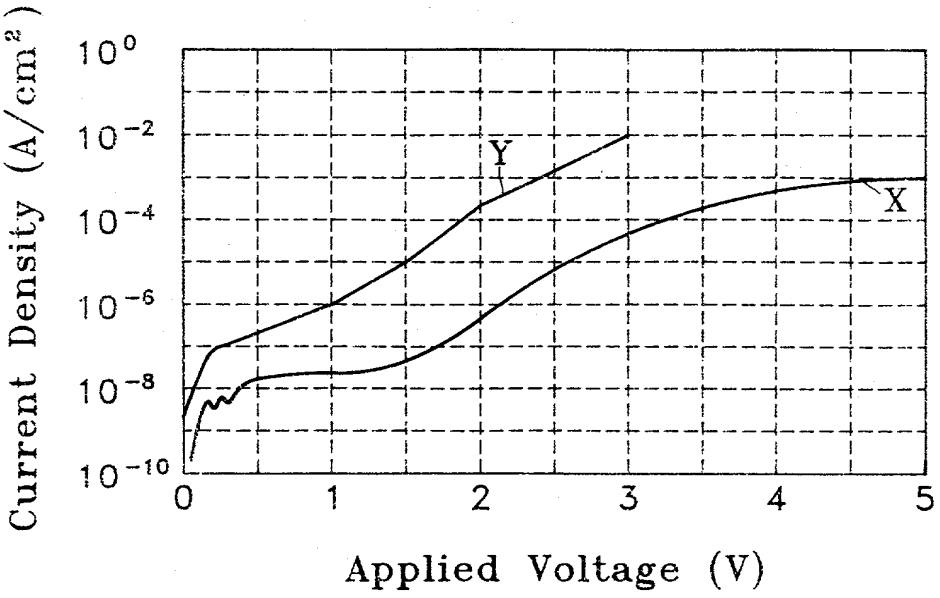

d1
d2
d3
TEST R

FIG.9


Current Density (A/cm²)
10⁰
10⁻²
10⁻⁴
10⁻⁶
10⁻⁸
10⁻¹⁰
0
1
2
3
4
5
Applied Voltage (V)
Y
X

Docket No.
647-1

Declaration and Power of Attorney For Patent Application

English Language Declaration

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

METHOD FOR FORMING LOWER ELECTRODE OF CAPACITOR

the specification of which

(check one)

☒ is attached hereto.

☐ was filed on _____ as United States Application No. or PCT International Application Number _____

and was amended on _____

(if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d) or Section 365(b) of any foreign application(s) for patent or inventor's certificate, or Section 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Not Claimed
95-13694	Rep. of Korea	May 29, 1995	☐
(Number)	(Country)	(Day/Month/Year Filed)	
			☐
(Number)	(Country)	(Day/Month/Year Filed)	
			☐
(Number)	(Country)	(Day/Month/Year Filed)	

I hereby claim the benefit under 35 U.S.C. Section 119(e) of any United States provisional application(s) listed below:

(Application Serial No.)	(Filing Date)

I hereby claim the benefit under 35 U. S. C. Section 120 of any United States application(s), or Section 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. Section 112. I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, C. F. R., Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

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Stephen R. Whitt	**34,753**	**William L. Geary, Jr.**	**35,879**
Allen LeRoy Limberg	**27,211**	**Brian C. Altmiller**	**37,271**

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Sole or first inventor's signature: Hwang, Cheol-sung Date: Nov. 10. 1995
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Full name of second inventor, if any
Second inventor's signature Date
Residence
Citizenship
Post Office Address

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT APPLICATION of　　　　　　　　　　Atty. Docket No.: SEC.314

HWANG, Cheol-Sung

Appln. Serial No.: 08/820,374
Filed: March 12, 1997
Title: Method for Forming Lower Electrode of Capacitor

ASSOCIATE POWER OF ATTORNEY

Hon. Assist. Commissioner
of Patents
Washington, D.C. 20231

Sir:

The undersigned attorney of record in this case hereby appoints **JONES & VOLENTINE, L.L.P.** and the below named persons, individually and collectively, as associate attorneys to prosecute this patent application and to transact all business in the United States Patent and Trademark Office connected therewith and with the resulting patent:

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BRIAN C. ALTMILLER, 37,271

Unless and until otherwise directed, please direct all communications about this application and the resulting patent to the above-appointed associate attorneys, at:

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The above-appointed associate attorneys are hereby authorized to act and rely on instructions from and communicate directly with the assignee of record, and with such patent agent/attorney liaison, individual or firm, selected by the assignee, as may represent themselves to the associate attorneys as having been so appointed, unless and until I instruct Jones & Volentine, L.L.P. in writing to the contrary.

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SAMSUNG ELECTRONICS CO., LTD.

Date: NOV. 5, 1997